Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A printhead controller, comprising:
a buffer circuit, for receiving an address signal and a selection signal, said buffer circuit outputting a buffer signal corresponding to said selection signal; and
an ink jetting circuit, for receiving said buffer signal and determining whether or not to jet out ink based on said buffer signal.

[c2] 2.The printhead controller of claim 1, wherein said address signal is a working driving voltage of said buffer circuit.

[c3] 3.The printhead controller of claim 1, wherein said buffer circuit includes a plurality of inverters connected in series.

[c4] 4. The printhead controller of claim 3, wherein each of said inverters includes a FET.

[c5] 5. The printhead controller of claim 4, wherein said buffer circuit includes:
a first resistor, having a first terminal for receiving said address signal;
a first FET, having a first terminal being coupled to a

second terminal of said first resistor and outputting an inverted signal, a second terminal for receiving said selection signal, and a third terminal being coupled to a ground;

a second resistor, having a first terminal for receiving said address signal; and

a second FET, having a first terminal being coupled to a second terminal of said second resistor and outputting said buffer signal, a second terminal for receiving said inverted signal, and a third terminal being coupled to said ground.

[c6] 6.The printhead controller of claim 5, wherein a resistance of said first resistor and said second resistor range from 0.5kΩ to 500kΩ.

[c7] 7.The printhead controller of claim 5, wherein a resistance of said first resistor and said second resistor range from 20kΩ to 80kΩ.

[c8] 8.The printhead controller of claim 4, wherein said buffer circuit includes:

a first FET, having a first terminal for receiving said address signal, a second terminal coupled to said first terminal of said first FET, and a third terminal for outputting an inverted signal;

a second FET, having a first terminal being coupled to

said third terminal of said first FET, and a second terminal for receiving saidselection signal;
a third FET, having a first terminal being coupled to a third terminal of said second FET, a second terminal for receiving a second selection signal, and a third terminal being coupled to a ground;
a fourth FET, having a first terminal for receiving said address signal, a secondterminal being coupled to said first terminal of said fourth FET, and a third terminal for outputting said buffer signal; and
a fifth FET, having a first terminal being coupled to said third terminal of said fourth FET, a second terminal for receiving said inverted signal, and a third signal being coupled to said ground.

[c9] 9.The printhead controller of claim 8, wherein said first FET is replaced by a first resistor, and saidfirst resistor has a first terminal for receiving said address signal and a second terminal being coupled to said first terminal of said second FET.

[c10] 10. The printhead controller of claim 8, wherein said second selection signal is said address signal.

[c11] 11. The printhead controller of claim 4, wherein said buffer circuit includes:
a first resistor, having a first terminal for receiving

said address signal;

a first FET, having a first terminal being coupled to a second terminal of said first resistor and outputting an inverted signal, a second terminal for receiving said selection signal, and a third terminal being coupled to a ground;

a second FET, having a first terminal for receiving said address signal, a second terminal being coupled to said first terminal of said second FET, and a third terminal for outputting said buffer signal; and

a third FET, having a first terminal being coupled to said third terminal of said second FET, a second terminal for receiving said inverted signal, and a third terminal being coupled to said ground.

[c12] 12.The printhead controller of claim 11, wherein a resistance of said first resistor ranges from 0.5kΩ to 500kΩ.

[c13] 13.The printhead controller of claim 11, wherein a resistance of said first resistor ranges from 20kΩ to 80kΩ.

[c14] 14.The printhead controller of claim 4, wherein said buffer circuit includes:

a first resistor, having a first terminal for receiving said address signal;

a first FET, having a first terminal being coupled to a second terminal of said first resistor and outputting an

inverted signal, a second terminal for receiving said selection signal, and a third terminal being coupled to a ground;

a second FET, having a first terminal for receiving said address signal, and a third terminal for outputting said buffer signal;

a third FET, having a first terminal being coupled to said first terminal and a second terminal of saidsecondFET, a second terminal and a third terminal being coupled to said third terminal of saidsecond FET; and

a fourth FET, having a first terminal being coupled to said third terminal of said second FET, a second terminal for receiving said inverted signal, and a third terminal being coupled to said ground.

[c15] 15.The printhead controller of claim 14, wherein a resistance of said first resistor ranges from 0.5kΩ to 500kΩ.

[c16] 16.The printhead controller of claim 14, wherein a resistance of said first resistor ranges from 20kΩ to 80kΩ.

[c17] 17. An ink jet printer, comprising:

a printhead drive unit, including a printhead drive circuit and a printhead selection circuit, said printhead drive circuit outputting a plurality of address signals, said printhead selection circuit outputting a plurality of selection signal; and

a plurality of printhead control units, each of said printhead control units receiving corresponding one of said plurality of address signals and corresponding one of said plurality of selection signals, each said printhead control unit including:

a plurality of buffer circuits, each of saidplurality of buffer circuits for receiving one of said address signals and one of said selection signals, each of saidplurality of buffer circuits outputting a buffer signal corresponding to saidreceived selection signal;

a plurality of ink jetting circuits, each of said plurality of ink jetting circuits for receiving buffer signal outputting from corresponding buffer circuit and determining whether or not to jet out ink based on said received buffer signal; and

a plurality of nozzles, each of said plurality of nozzles corresponding to one of said plurality of ink jetting circuits for jetting out said ink.

[c18] 18.The ink jet printer of claim 17, wherein said address signal is a working driving voltage of said buffer circuit.

[c19] 19.The printhead controller of claim 17, wherein each of said buffer circuits includes a plurality of inverters serial-connected to each other.

[c20] 20. The printhead controller of claim 19, wherein each of

said invertersincludes a FET.